the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

The Official Action rejects claims 8, 14 and 16 as obvious based on the combination of U.S. Patent No. 6,841,433 to Seo and U.S. Patent No. 6,777,286 to Clevenger. It appears that the rejection of claims 14 and 16 relates to these claims as they depend, either directly or indirectly, from independent claim 8. The Applicant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claim 8 recites, among other features, heat-treating a semiconductor film and a first insulating film; patterning the semiconductor film and the first insulating film into island shapes with the use of the

same photomask after heat-treating the semiconductor film and the first insulating film to form an island-shaped semiconductor film and an island-shaped gate insulating film; forming a second insulating film over the island-shaped gate insulating film; and etching the second insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film and the island-shaped gate insulating film in self-aligned manner. In other words, claim 8 recites (1) heating a first insulating film (which is later patterned to form an island-shaped gate insulating film) for patterning a semiconductor and the first insulating film; (2) patterning the semiconductor film and the first insulating film by the same photomask; and (3) forming a second insulating film over the first insulating film (island-shaped gate insulating film); and etching the second insulating film to form a side wall covering sides of the semiconductor and the first insulating film (island-shaped gate insulating film). For the reasons provided below, Seo and Clevenger, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Official Action asserts that "Seo et al. disclose a method for manufacturing a thin film transistor where a semiconductor film (102) is formed over an insulating substrate (100); forming a first insulating film (104) over the semiconductor film (102); heat-treating the semiconductor film and the first insulating film (Fig. 3B, col. 6, lines 37-49); patterning the semiconductor film (102) and the first insulating film (106) into island shapes (107) with the use of the same photomask after heat-treating the semiconductor film and the first insulating film to form an island-shaped semiconductor film and an island-shaped gate insulating film (107)" (pages 2-3, Paper No. 03202006; emphasis added).

The Official Action concedes that "Seo et al. do not disclose forming a second insulating film over the island-shaped gate insulating film; etching the second insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film and the island-shaped gate insulating film in self-aligned manner" (page 3, Id.) However, the Applicant respectfully submits that Seo also does not

disclose (1) heating a first insulating film (which is later patterned to form an island-shaped gate insulating film) for patterning a semiconductor and the first insulating film; and (2) patterning the semiconductor film and the first insulating film by the same photomask.

Specifically, as noted above, the Official Action asserts that Seo teaches "a semiconductor film (102) ... a first insulating film (104) ... the first insulating film (106) ... and an island-shaped gate insulating film (107)" (pages 2-3, Id.). However, Seo teaches a buffer layer 102, an amorphous silicon layer 104, a polycrystalline silicon layer 106, an island pattern 107, and a gate insulation layer 110 (column 6, line 30, to column 7, line 44; and Figures 3B-3F, 4A and 4B, reproduced below).

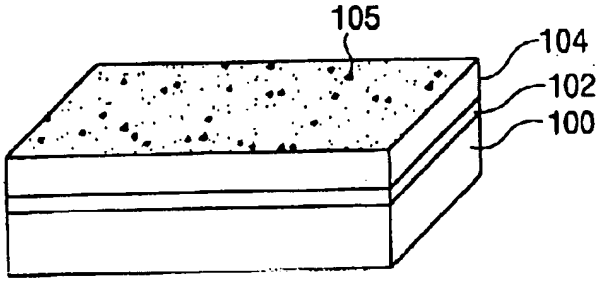

FIG. 3B

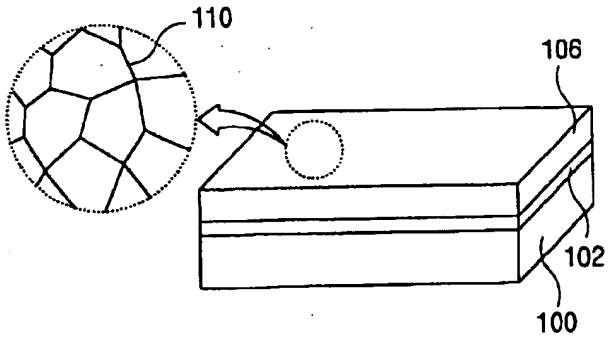

FIG. 3C

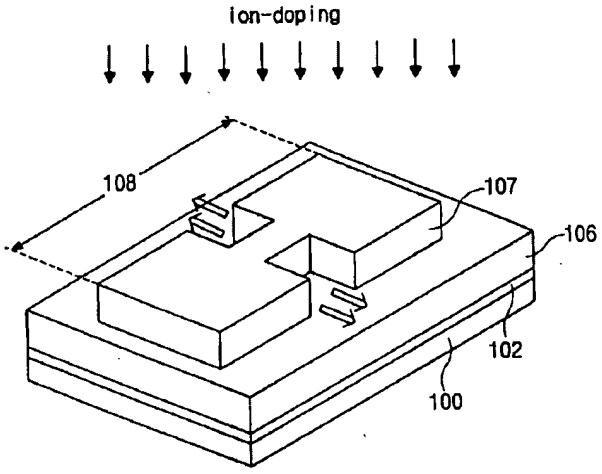

FIG. 3D

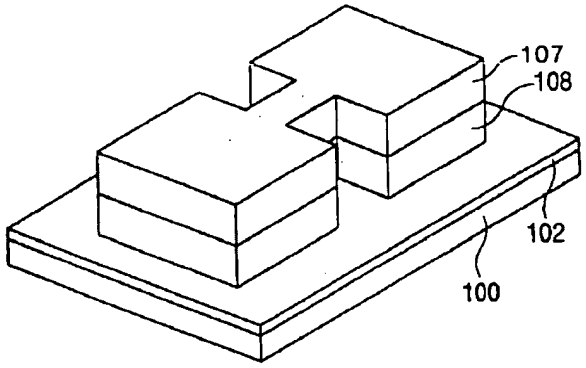

FIG. 3E

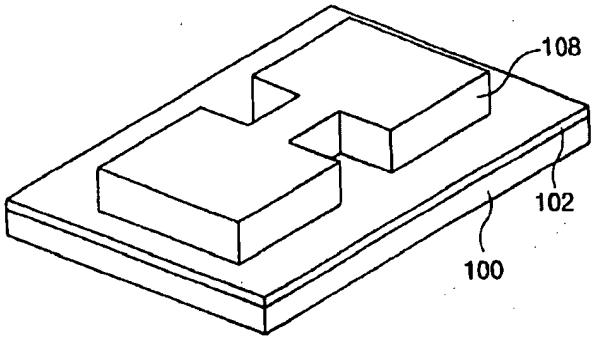

FIG. 3F

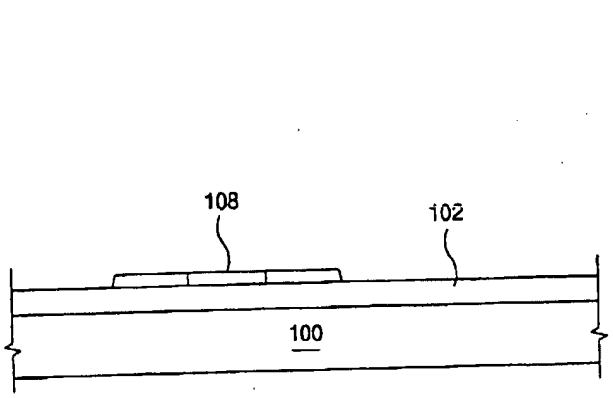

FIG. 4A

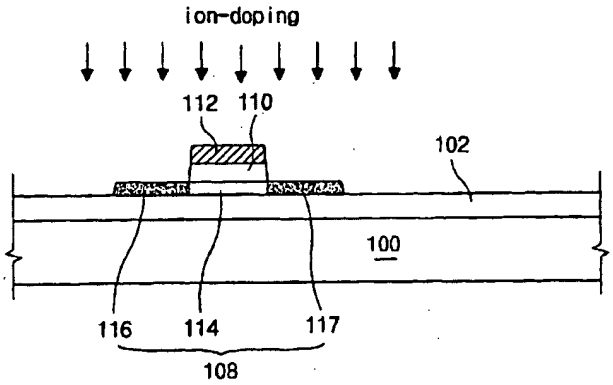

FIG. 4B

That is, in Seo, the semiconductor film is not buffer layer 102 as asserted in the Official Action, but might correspond with amorphous silicon layer 104. Also, in Seo, the first insulating film (later an island-shaped gate insulating film) is not amorphous silicon layer 104 or polycrystalline silicon layer 106 as asserted in the Official Action. Further, in Seo, the island-shaped gate insulating film in Seo is not the island pattern 107 as asserted in the Official Action. Rather, Seo appears to teach a gate insulation film 110 formed on active layer 108 (column 7, lines 34-35; Figure 4B). Still further, Seo does not teach or suggest heating a gate insulating film (presumably 110 in Figure 4B) before patterning a semiconductor film. Even further, Seo does not teach or suggest patterning a semiconductor film (presumably 104 in Figure 3B or 106 in Figure 3C) and a gate insulating film (presumably 110 in Figure 4B) by a same mask.

Therefore, Seo does not teach or suggest (1) heating a first insulating film (which is later patterned to form an island-shaped gate insulating film) for patterning a semiconductor and the first insulating film; (2) patterning the semiconductor film and the first insulating film by the same photomask; and (3) forming a second insulating film over the first insulating film (island-shaped gate insulating film); and etching the second insulating film to form a side wall covering sides of the semiconductor and the first insulating film (island-shaped gate insulating film). As such, Seo does not teach or suggest heat-treating a semiconductor film and a first insulating film; patterning the semiconductor film and the first insulating film into island shapes with the use of the same photomask after heat-treating the semiconductor film and the first insulating film to form an island-shaped semiconductor film and an island-shaped gate insulating film; forming a second insulating film over the island-shaped gate insulating film; and etching the second insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film and the island-shaped gate insulating film in self-aligned manner.

Clevenger does not cure the deficiencies in Seo. The Official Action asserts that Clevenger teaches that "a semiconductor film (10) is formed over an insulating substrate [(20)]; patterning the semiconductor film (10) to form an island-shaped semiconductor film; forming an insulating film (80) over the island-shaped gate insulating film; etching the insulating film anisotropically to form a side wall (70) covering side faces of the island-shaped semiconductor film in self-aligned manner; forming a conductive film (85) over the island-shaped gate insulating film after forming the side wall; and patterning the conductive film to form a gate electrode (col. 5, lines 43-59)" (page 3, Paper No. 03202006; emphasis added).

However, Clevenger does not teach or suggest forming a second insulating film over the first insulating film (island-shaped gate insulating film); and etching the second insulating film to form a side wall covering sides of the semiconductor and the first insulating film (island-shaped gate insulating film). Initially, it is noted that the

specification of Clevenger does not provide any detail regarding reference character 80 in Figure 2 (Figures 1-3 reproduced below).

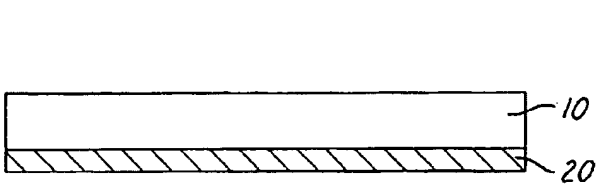

FIG. 1

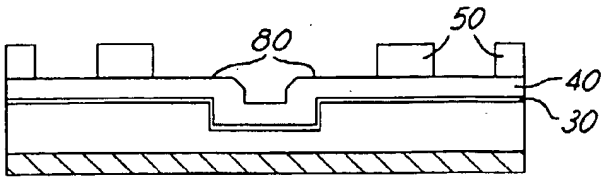

FIG. 2

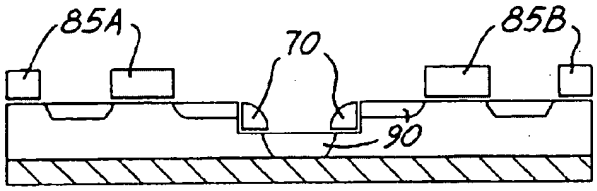

FIG. 3

Clevenger appears to teach a SOI substrate silicon 10 on buried oxide layer 20, gate oxide layer 30, gate conductor material 40 and mask 50 used to form pull-down gate regions 85A and 85B and transfer devices 70 (column 5, lines 43-59). Reference character 80 appears to refer to a trench region of gate conductor material 40, and not to an insulating film. In any event, Clevenger does not teach or suggest etching an insulating film to form a side wall. Also, Clevenger does not teach or suggest that a side wall, which is formed by etching, covers a side face of a gate insulating film. Therefore, Clevenger does not teach or suggest (3) forming a second insulating film over the first insulating film (island-shaped gate insulating film); and etching the second insulating film to form a side wall covering sides of the semiconductor and the first insulating film (island-shaped gate insulating film).

Further, Clevenger does not teach or suggest (1) heating a first insulating film (which is later patterned to form an island-shaped gate insulating film) for patterning a semiconductor and the first insulating film; (2) patterning the semiconductor film and the first insulating film by the same photomask.

Therefore, Seo and Clevenger, either alone or in combination, do not teach or suggest heat-treating a semiconductor film and a first insulating film; patterning the semiconductor film and the first insulating film into island shapes with the use of the same photomask after heat-treating the semiconductor film and the first insulating film to form an island-shaped semiconductor film and an island-shaped gate insulating film; forming a second insulating film over the island-shaped gate insulating film; and etching the second insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film and the island-shaped gate insulating film in self-aligned manner.

Since Seo and Clevenger do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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Reg. No. 53,470

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